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contact pads for the back side of the chip which are exposed by the preferential etching away of the silicon. - -

Please amend the paragraph [0010] beginning at page 4, line 13 to read as follows:

-- [0010] One of the problems with using silicon based structures for electronic packaging applications is to be able to provide a highly reliable product by employing an efficient method of forming vias through a membrane thin silicon substrate, i.e. from the bottom surface through the silicon to the top of the silicon where the wiring structure is fabricated. That requires forming the vias without breaking the fragile membrane thin wafer and yet performing the task with a highly competitive manufacturing cost. - -

IN THE CLAIMS

1. (Amended) A method for fabricating a silicon based package (SBP) in the sequence as follows:

starting with a wafer composed of silicon and having a first surface and a reverse surface which are planar as the base for the SBP,

then forming an interconnection structure including multilayer conductor patterns over the first surface,

then forming a protective overcoat layer over the interconnnection structure,

then forming a temporary bond between the protective overcoat layer of the SBP and a wafer holder, with the wafer holder being a rigid structure,

then thinning the reverse surface of the wafer to a desired thickness to form an ultra thin silicon wafer (UTSW) for the SBP,

then forming via holes which extend through the UTSW, and

then forming metallization in the via holes with the metallization extending through the UTSW.

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14. (Amended) A method for fabricating a silicon based package (SBP) comprising:

providing a base for the SBP comprising a wafer composed of silicon and having a first surface and a reverse surface which are planar,

then forming via holes which extend partially through the wafer from the first surface towards the reverse surface with the each via hole having a base thereof which is closest to the reverse surface,

then forming a dielectric layer covering the first surface of the silicon wafer and the via holes with distal portions of the dielectric layer being located at the bases of the via holes, so that the distal portions are closest to the reverse surface,

then forming metal vias in the via holes on the dielectric layer with proximal ends being located at the first surface and distal ends of the metal vias being located on the distal portions of the dielectric layer, thereby being closest to the reverse surface,

then forming an interconnection structure including multilayer conductor patterns over the metal vias and th e dielectric layer,

then forming a protective overcoat layer over the interconnnection structure,

then forming a temporary bond between the protective overcoat layer of the SBP and a wafer holder, with the wafer holder being a rigid structure leaving the reverse surface of the wafer exposed,

then thinning the reverse surface of the wafer to a desired thickness to form an ultra thin silicon wafer (UTSW) for the SBP exposing the distal portions of the dielectric layer covering the distal ends of the metal vias, and

then removing the distal portions of the dielectric layer exposing the distal ends of the metal vias which extend through the UTSW.

Cancel claims 17-24 without prejudice to prosecution thereof in a divisional application.

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Add the following claims:

25. A method for fabricating a Silicon Based Package (SBP) in the sequence as follows:

starting with a wafer composed of silicon and having a first surface and a reverse surface which are planar as the base for the SBP,

then forming an interconnection structure including multilayer conductor patterns over the first surface,

then forming a protective overcoat layer composed of polyimide over the interconnnection structure,

then forming a temporary bond between the protective overcoat layer of the SBP and a wafer holder, with the wafer holder being a rigid structure,

then thinning the reverse surface of the wafer to a desired thickness to form an Ultra Thin Silicon Wafer (UTSW) for the SBP,

then forming via holes which extend through the UTSW, and

then forming metallization in the via holes with the metallization extending through the UTSW.

26. The method of claim 25 including:

forming the temporary bond with polyimide, and

releasing the temporary bond by laser ablation.

27. A method for fabricating a silicon based package (SBP) comprising:

providing a base for the SBP comprising a wafer composed of silicon and having a first surface and a reverse surface which are planar,

then forming via holes which extend partially through the wafer from the first surface towards the reverse surface with the each via hole having a base thereof which is closest to the reverse surface,